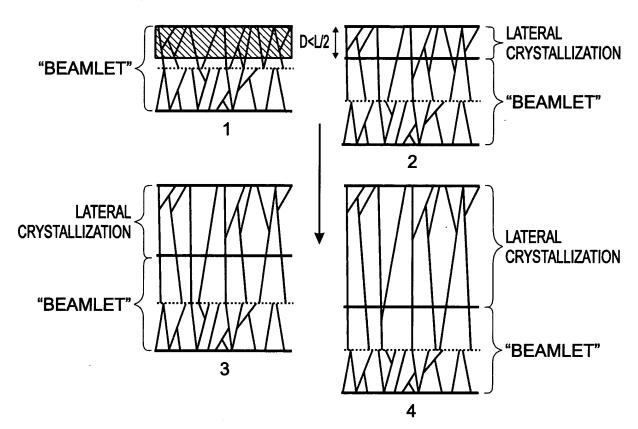
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Fig. 1 (PRIOR ART)



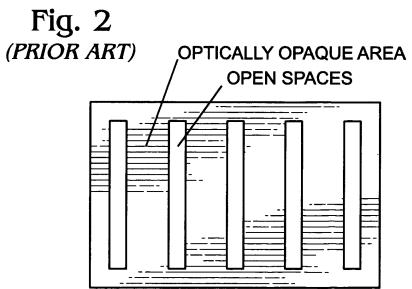
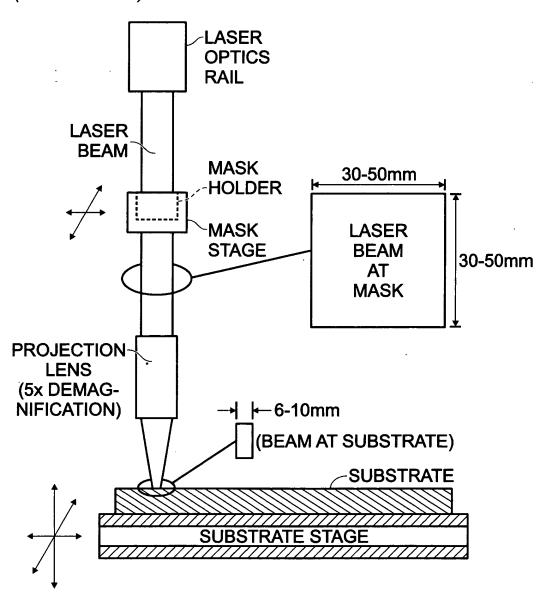
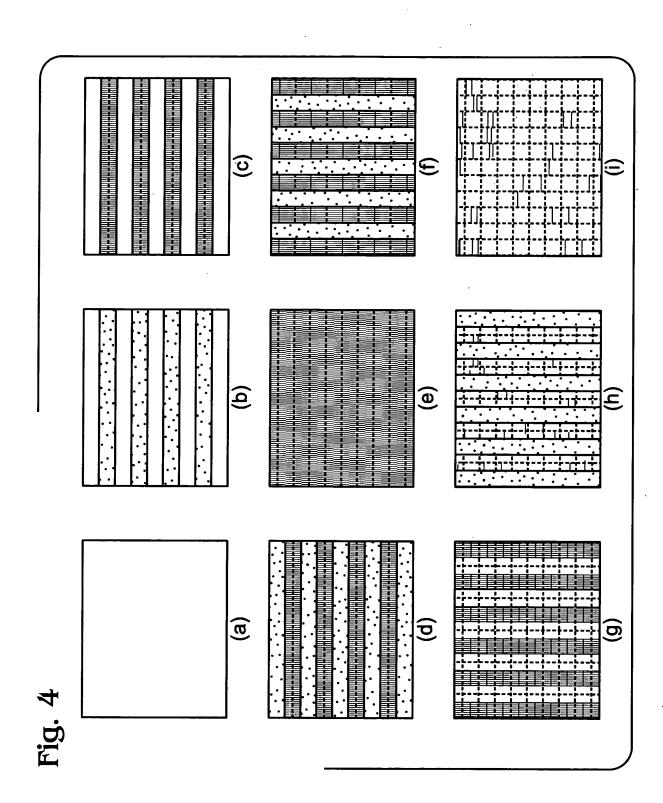


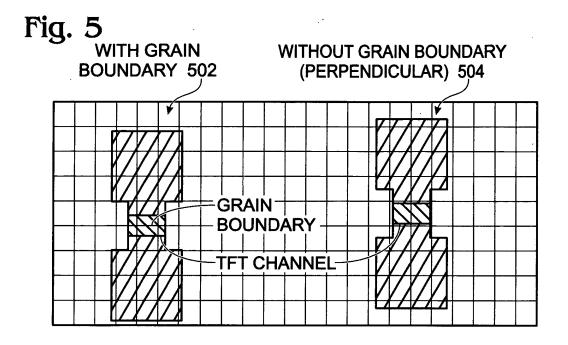
Fig. 3 (PRIOR ART)

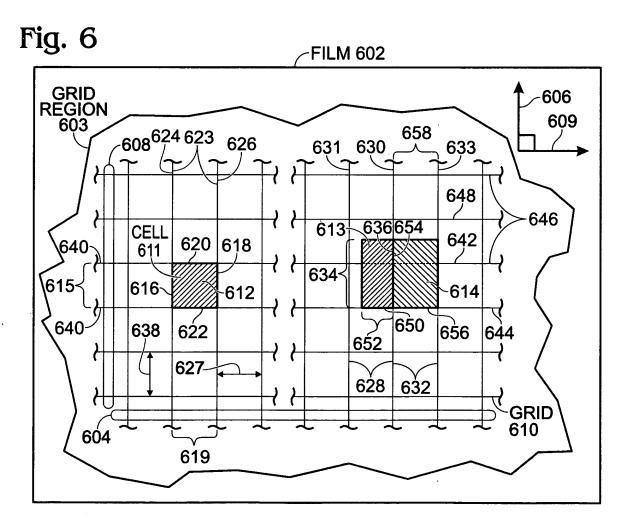


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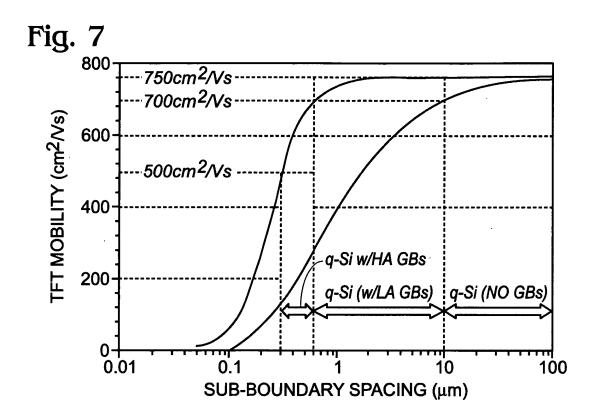


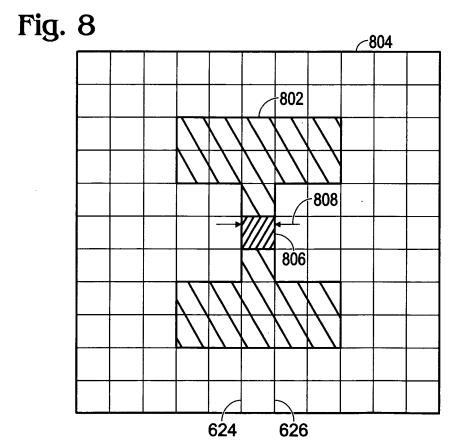
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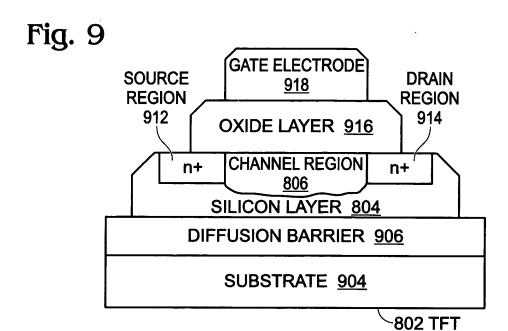


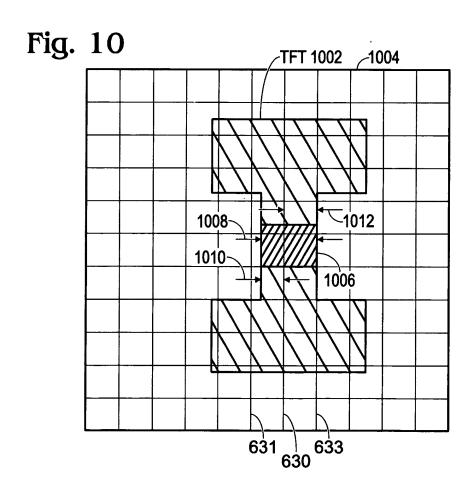


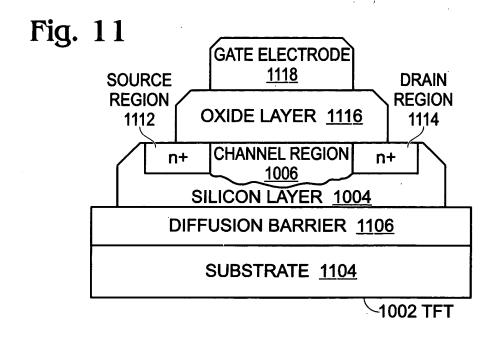
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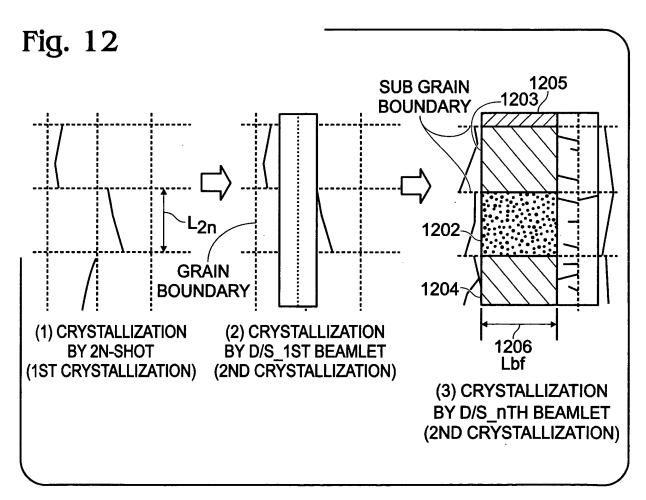


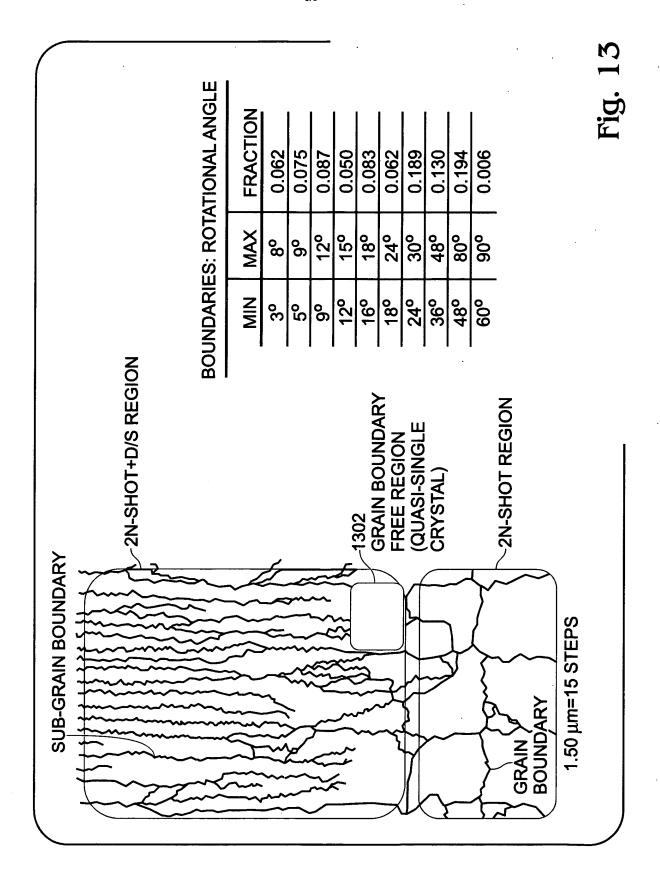












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Fig. 14		1400
пп20° и и	(ST/	ART
		1401
	-ORMING A TRANSPAR	ENT SUBSTRATE LAYER
		1402
	FORMING A DIFF	FUSION BARRIER
		1403
	FURINING A FILIVI OF A	AMORPHOUS SILICON
	ZA LTOUS IAC A SIAISIL	₹ PROCESS TO FORM
		LLINE SILICON
	7	¹ √1407
EXPOSING	THE FIRST AREA TO A	N ADDITIONAL ENERGY SOURCE
		1410
		R BEAM, IN TWO STEPS PER
IIEKAI	PATTERNS AND ANNE	RST AND SECOND APERTURE ALING THE FIRST AREA
	777777777777777777777777777777777777777	1414
FORMING,	IN THE FIRST AREA, O	RTHOGONAL FIRST AND SECOND
		RIDGED, GRAIN BOUNDARIES
	7	1416
SELECT	TING A SECOND AREA,	INCLUDED IN THE FIRST AREA
	7	141 <u>8</u>
USING DIRE	CTIONAL SOLIDIFICATI	ON TO ANNEAL THE SECOND AREA
		<u>/1419</u>
EXPOSING T	THE SECOND AREA TO	AN ADDITIONAL ENERGY SOURCE
	7	/
USING A	LASER TO SEQUENTIA	LLY ANNEAL THE SECOND AREA
	(55.40) (41.0 65.41)	1424
SELECTIVELY	Y REMOVING GRAIN BOI	UNDARIES AND SMOOTHING RIDGES
EOD (4)	TO A TOUR A TOUR A OLD	1426
L FORMI	ING A TRANSISTOR CHA	ANNEL IN THE SECOND AREA
FORMIN	IG SOURCE AND DRAIN	REGIONS IN THE FIRST AREA
		7 /1430
	FORMING A GATE I	DIELECTRIC LAYER
	, , , , , , , , , , , , , , , , , , ,	7 /1432
FORMING A	GATE ELECTRODE OV	ERLYING THE DIELECTRIC LAYER